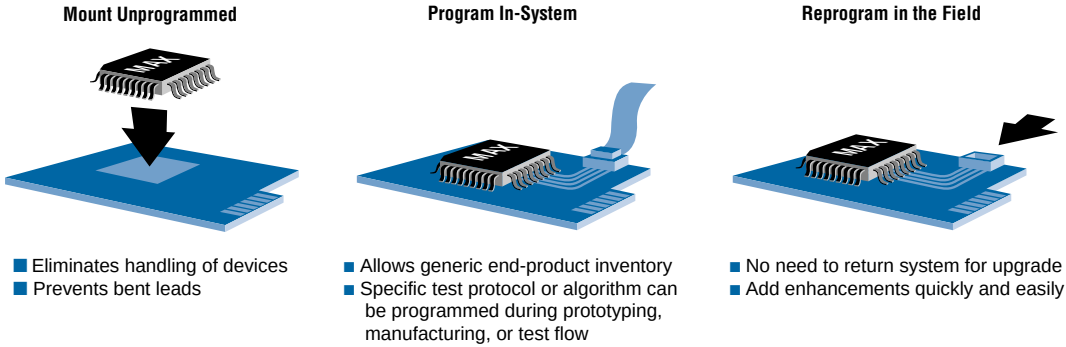
Introduction to ISP

February 1998, ver. 3

The in-system programmability (ISP) feature facilitates prototyping during design development, streamlines manufacturing, and increases design flexibility. ISP also enables quick and efficient upgrades in the field.

The ISP feature—available in MAX® 9000 (including MAX 9000A), MAX 7000S, and MAX 7000A devices—uses the IEEE Std. 1149.1 Joint Action Test Group (JTAG) test port. This process allows devices to be programmed and the printed circuit board (PCB) to be functionally tested in a single manufacturing step, saving testing times and assembly costs. See Figure 1.

Figure 1. ISP Increases Manufacturing Efficiency



Whether you are using Altera's ByteBlaster™ parallel port or BitBlaster™ serial download cable during prototyping, in-circuit testers during manufacturing, or an embedded processor for field upgrades, Altera's ISP-capable devices and support provide an industry-standard solution for all types of applications.

The Jam™ programming and test language addresses the issues designers face when programming programmable logic devices (PLDs) in-system. These issues include proprietary file formats, vendor-specific programming algorithms, large file sizes, and long programming times. The Jam language is a major step forward in providing a software-level standard for in-system programming.

For more information on the Jam language, see *Product Information Bulletin 27 (Jam Programming & Test Language Overview)* and the *Jam Programming & Test Language Specification, version 1.1* in this handbook.

MAX 9000 Devices

The high-density MAX 9000 family, which includes the original MAX 9000 devices and the new high-speed MAX 9000A devices, provides innovative solutions for today's design challenges. By offering a wide variety of advanced system-level features—such as ISP, built-in JTAG boundary-scan test (BST) support, and MultiVolt™ I/O capability—the MAX 9000 family addresses critical design challenges at the device level.

The MAX 9000 family builds on the success of Altera's popular MAX 7000 family, while offering higher densities and maintaining the industry's highest performance. Ranging from 320 to 560 macrocells (6,000 to 12,000 usable gates), the MAX 9000 family has propagation delays from 7.5 to 20 ns and typical in-system performance of 70 MHz. In addition, each MAX 9000 device package is function- and pin-compatible with all other MAX 9000 device packages. This compatibility makes it easy to migrate designs from one density level to another while maintaining pin assignments, eliminating the need for board layout changes. Table 1 lists benefits of MAX 9000 devices.

Table 1. MAX 9000 Benefits

Feature	Benefit
ISP	Easy prototyping Permits in-field upgrades Simplifies the manufacturing flow
6,000 to 12,000 usable gates and 320 to 560 macrocells	Improves system integration Ideal for gate-array prototyping
7.5-ns propagation delays	Increases in-system performance to 178 MHz
MultiVolt I/O operation	Ideal for mixed-voltage systems
Built-in JTAG support	Simplifies device and system testing

For more information about MAX 9000 devices, go to the *MAX 9000 Programmable Logic Device Data Sheet* later in this handbook.

MAX 7000S Devices

Ranging from 32 to 256 macrocells (600 to 5,000 usable gates), MAX 7000S devices are ideal for system-level integration. Altera's MAX 7000S devices feature ISP, and devices with 128 or more macrocells have built-in JTAG BST circuitry. The enhanced MAX 7000S devices feature six global output enable signals, two global clocks, fast input registers, and programmable slew-rate control.

These enhanced features enable MAX 7000S devices to address a broad range of system-level applications. For example, the six logic- or pin-controlled output enable signals allow direct connection to multiple buses found in microprocessor controlled systems. The two high-speed global clocks provide increased flexibility. The fast setup times enable high-speed device-to-device communication.

Additionally, the programmable output slew-rate control helps reduce system noise by slowing the switching time of non-speed-critical outputs. A programmable power-saving feature allows for 50% or greater power reduction in each macrocell. Table 2 lists the benefits of MAX 7000S devices.

Table 2. MAX 7000S Benefits

Feature	Benefit
ISP	Easy prototyping Permits in-field upgrades Simplifies manufacturing flow
600 to 5,000 usable gates	Multiple density options.
32-macrocell, 44-pin devices to 256-macrocell, 208-pin devices	High pin-to-logic ratios for a wide variety of applications.
5-ns propagation delays	Provides over 175-MHz counter frequencies.
Built-in JTAG support	Simplifies device and system testing.
Programmable power-saving mode	Enables greater than 50% power reduction.
MultiVolt I/O operation	Ideal for mixed-voltage systems.
Peripheral component interconnect (PCI) compliance	Satisfies PCI bus requirements.

For more information about MAX 7000S devices, go to the *MAX 7000 Programmable Logic Device Data Sheet* later in this handbook.

MAX 7000A Devices

The high-density, high-performance MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 20,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 178.6 MHz. These devices range from 32 to 1,024 macrocells, and they are function-, pin-, and Jam File-compatible with the industry-standard MAX 7000 family, making them ideal for system-level integration. MAX 7000A devices include enhanced features such as 6 to 10 pin- or logic-driven output enable signals, two global clock signals with optional inversion, enhanced interconnect resources for improved routability, fast input setup times, and a programmable output slew-rate control.

In addition, MAX 7000A devices provide programmable speed/power optimization, which enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V and all input pins are 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems. Table 3 lists the benefits of MAX 7000A devices.

Table 3. MAX 7000A Benefits

Feature	Benefit
ISP	Easy prototyping Permits in-field upgrades Simplifies manufacturing flow
600 to 20,000 usable gates	Multiple density options.
32-macrocell, 44-pin devices to 1,024-macrocell, 256-pin devices	High pin-to-logic ratios for a wide variety of applications.
5-ns propagation delays	Provides over 175-MHz counter frequencies.
Built-in JTAG support	Simplifies device and system testing.
Programmable power-saving mode	Enables greater than 50% power reduction.
MultiVolt I/O operation	Ideal for mixed-voltage systems.
PCI compliance	Satisfies PCI bus requirements.

For more information about MAX 7000A devices, go to the *MAX 7000 Programmable Logic Device Data Sheet* later in this handbook.

Conclusion

Using ISP can lengthen the life and enhance the quality and flexibility of the end product, as well as reduce device inventories by eliminating the need to stock and track programmed devices. ISP can achieve prototyping during design development, streamline manufacturing , and increase design flexibility easily. ISP also enables quick and efficient field upgrades, and allows devices to be programmed and the PCB to be functionally tested in a single manufacturing step, saving testing times and assembly costs.